FDTD MODELING OF SWITCHING NOISE IN MULTI-LAYERED DIGITAL CIRCUITS WITH CMOS INVERTERS AND PASSIVE LUMPED ELEMENTS

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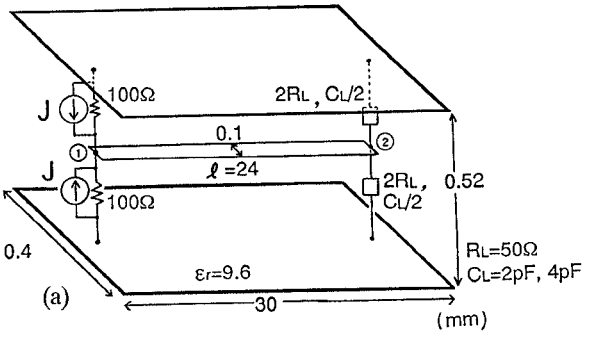
ABSTRACT

Multi-layered digital circuits such as LSI packages, has been analyzed by using a Finite-Difference Time-Domain (FDTD) method. Linear lumped elements, resistors and capacitors, and nonlinear lumped elements, CMOS drivers, are included in the analyses. Various noises as well as digital pulse propagation in multi-layered circuits are effectively analyzed by this technique.

INTRODUCTION

In LSI packages and MCMs(Multi-Chip Module), the distributed circuit properties of the circuits become remarkable with increasing the digital clock speed. Furthermore, the switching devices tend to yield various electric noises such as ground bounce, crosstalk, EMI noise which leads to a system malfunction [1][2][3]. Although several papers have shown the efficiency of the FDTD method combined with lumped circuit elements [4][5] for analyzing high speed digital propagation in three dimensional digital circuits, the switching noise has not been analyzed.

This paper analyses the signal propagation as well as switching noises in the three dimensional multi-layered circuit by using the FDTD method combined with lumped circuit elements. In the analysis, the lumped elements such as CMOS inverters, resistors, and capacitors are implemented in distributed circuit structures and inclusive electromagnetic phenomena in the high-speed digital circuit systems are simulated.



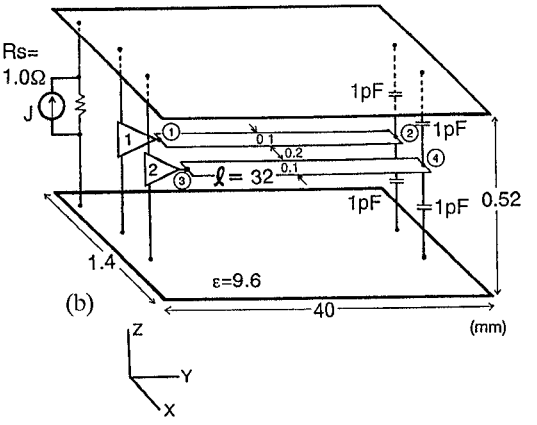


Fig.1 (a) Stripline configuration analyzed for verification of passive lumped elements. The characteristic impedance of the line is 50Ω. The grid counts are 40, 50, 20 for x, y, z directions. (b) Multi-layered circuit analyzed with CMOS inverters and lumped capacitors. The characteristic impedance of each line is 50Ω. The grid counts are 50, 70, 20 for x, y, z directions.

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NUMERICAL ANALISYS

Two types of circuits are analyzed; the ideal stripline with lumped capacitors or resistors in Fig.1(a), and the biased stripline with lumped CMOS inverters and capacitive loads in Fig.1(b).

A. Analysis of Lumped Capacitor and Resistor

The lumped circuit elements are defined at the electric field nodes in the Yee's grid [6] as in refs. [4][5]. The current density through transistors J_{tr}, resistors J_R, and capacitors J_C are added to the Ampere's law as

$$\text{rot}\, H = \varepsilon \frac{\partial E}{\partial t} + \sigma E + J_{tr} + J_R + J_C, \qquad (1)$$

$$J_R = \sigma_R E, \qquad (2)$$

$$J_C = \varepsilon_C \frac{\partial E}{\partial t}. \qquad (3)$$

where σ_R and ε_C denote the effective conductance and the effective dielectric constant determined from the size of the grids where the lumped elements are defined.

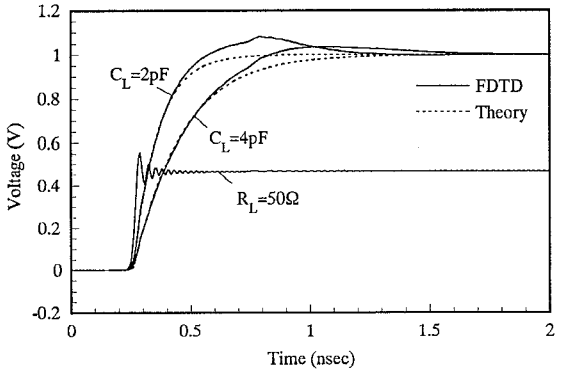

Fig.2 Time response of the passive lumped elements in Fig.1(b). The raising time of the input pulse is 20 psec. The dotted line is the theoretical value for capacitors.

To validate the response of the elements, digital pulse propagation in a stripline is analyzed with lumped element termination. The capacitive or resistive element is loaded at one end of 50Ω stripline as shown in Fig.1(a). And a raised cosine type step pulse with raising time of 20 psec is used for excitation. The FDTD results shown in Fig.2 demonstrate that overshoots are occurred in case of the capacitive loads which can be attributed to parasitic inductances of the termination. The result for the resistive 50Ω termination shows ringing caused by a dispersion of the stripline.

B. Implementation of CMOS Inverter

The equivalent circuit shown in Fig.3 is adopted for the CMOS inverter model. The implemented drain current of the N-type transistor as the function of gate-source voltage V_{gs}, drain-source voltage V_{ds}, and threshold voltage V_t is given by

$$I_d = \begin{cases} 0, & \text{for } V_{gs} - V_t \le 0, \\ \beta\,(V_{gs} - V_t)^2 (1 + \lambda V_{ds}), & \text{for saturation region,} \\ & V_{ds} \ge V_{gs} - V_t > 0, \\ \beta V_{ds} \{2\,(V_{gs} - V_t) - V_{ds}\} (1 + \lambda V_{ds}), & \text{for linear region,} \\ & V_{gs} - V_t > V_{ds} \ge 0, \end{cases} \qquad (4)$$

where β and λ denote the transconductance parameter and the channel length modulation, respectively [7]. For a P-type transistor, I_d, V_{ds}, V_{gs}, and V_t in (4) are replaced by $-I_d$, $-V_{ds}$, $-V_{gs}$, and $-V_t$. This model is equivalent to the level-1 model of SPICE. The static I_d vs. V_{ds} characteristics of the implemented CMOS inverter are shown in Fig.4 together with those of SPICE level-1 model. Curves for FDTD and SPICE agree well with each other. The operating points of CMOS inverters V_{ds}, and I_d are solved by using Newton method. This algorithm remains stable because the time increment of the FDTD algorithm is sufficiently smaller than the transition time of the CMOS inverters.

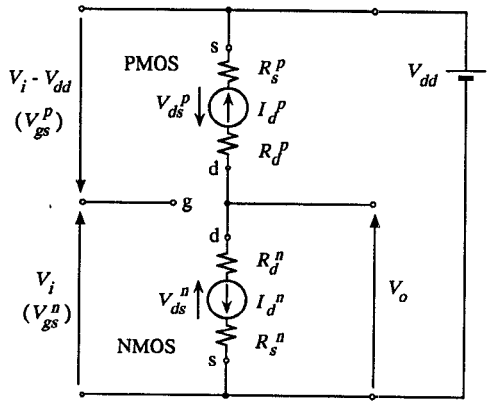

Fig.3 Equivalent circuit for the implemented CMOS inverter model. The source and drain ohmic resistances $R_s = R_d = 5\Omega$, the transconductance parameter $\beta = 0.003A/V^2$, the channel length modulation $\lambda = 0.02$ for both N and P type transistors, and the threshold voltage $V_t^n = -V_t^p = 1.0V$.

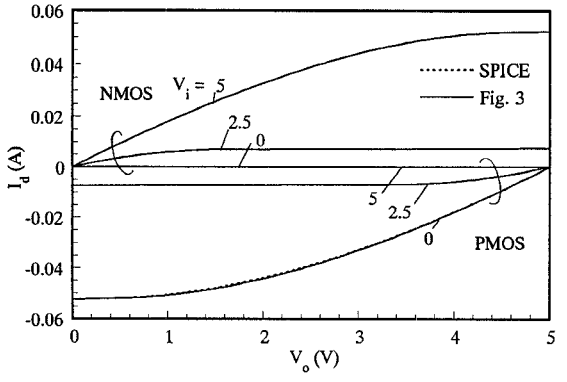

Fig.4 The static I_d vs. V_{ds} characteristics of the implemented CMOS inverter together with those of SPICE level-1 model. V_o denotes the output voltage of the inverter as shown in Fig.3. Curves for FDTD and SPICE agree well with each other.

RESULTS AND DISCUSSION

The CMOS inverters are connected between the power and ground plane of the stripline as shown in Fig.1(b) to generate the digital switching pulse. The characteristic impedance of each line is 50Ω, and loading capacitances of 1pF is connected from each line to power and ground plane. A bias voltage is applied with current sources whose source resistance is

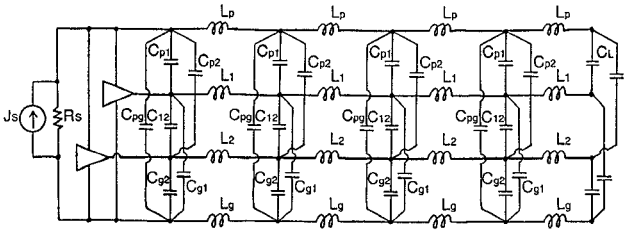

Fig.5 The stripline modeled as a four-stair ladder circuit for SPICE simulation. The parameter L, C are extracted with a commercial software "Parasitic Parameters" which is for three-dimensional structure analysis. J_s =1A, R_s =1Ω, $L_p = L_g$ = 0.4nH, $L_1 = L_2$ =4.2nH, $C_{p1} = C_{p2} = C_{g1} = C_{g2}$ =0.63pF, C_{12} =0.21pF, C_{pg} =1.0pF, C_L =1.0pF.

1Ω. Switching is occurred only at the inverter-1 after the bias voltage between the power and ground plane settled whereas the inverter-2 remains quiet.

The stripline in Fig.1(b) was also analyzed by using SPICE to compare the results with those of FDTD analysis. The transmission line parameters L, C used in the SPICE circuit were extracted with a commercial software "Parasitic Parameters"[8]. The stripline is modeled as a four-stair ladder circuit as shown in Fig.5.

The voltage of the power plane V_{bias}, which is obtained by integrating the electric field from ground to power plane at the CMOS inverter, is shown in Fig.6(a). A voltage fluctuation, called switching noise is observed in the FDTD result. The switching noise is owing to a switching current of the inverter flowing though the parasitic inductance of the plane between the bias point and the CMOS inverter. In case of the SPICE result, only small switching noise is observed because the parasitic inductance of the plane is not modeled. The voltage V_2 and V_4 for the resultant pulse waveforms at each receiving end of the lines are shown in Fig.6(b) and (c). There are differences between the results of FDTD and SPICE. Especially V_4 for the FDTD result in (c), one can observe the crosstalk noise which is over three times larger than that for the SPICE result. This will be resulted because small and complicated mutual coupling elements are neglected in SPICE cirquit.

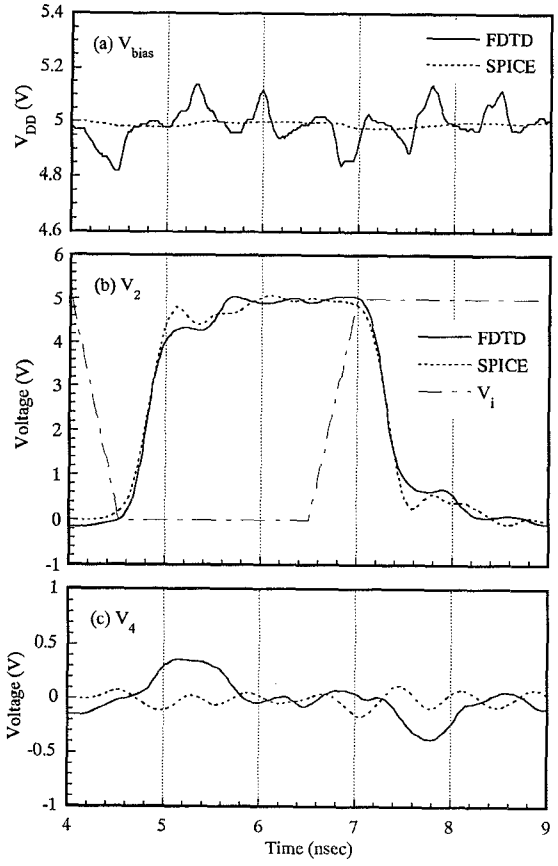

Fig.6 Resultant wave forms of FDTD and SPICE analysis observed at the power plane (a), and at the receiving end of the active line (b) and the quiet line (c). The broken thin line in (b) shows the input pulse entered into the CMOS inverter.

CONCLUSION

The FDTD technique combined with CMOS inverters and passive lumped circuit elements has been discussed. For the analyses of noise and pulse wave propagation in the 3D structure circuits such as LSI packages and MCMs, it is found that this technique enables accurate analysis with inclusive electromagnetic phenomena in complicated multi-layered circuits.

REFERENCES

[1] G.A.Katopis, "Delta-I Noise Specification for a High-Performance Computing Machine,"*Proc. of the IEEE*, vol.73, pp.1405-1415, 1985.

[2] W.D.Becker, P.H.Harms and R.Mittra, "Time-Domain Electromagnetic Analysis of Interconnects in a Computer Chip Package," *IEEE Trans. Microwave Theory Tech.*, vol.40, pp.2155-2163, 1992.

[3] R.Mittra, S.Chebolu and W.D.Becker, "Efficien Modeling of Power Plane in Computer Packages Using the Finite Difference Time Domain Method,"*IEEE Trans. Microwave Theory Tech.*, vol.42, pp.1791-1795, 1994.

[4] W.Sui, A.Christensen, and C.H.Durney, "Extending the Two-Dimensional FDTD Method to Hybrid Electromagnetic Systems with Active and Passive Lumped Elements," *IEEE Trans. Microwave Theory Tech.*, vol.40, pp.724-730, 1992.

[5] M.Piket-May, A.Taflove, and J.Baron, "FD-TD Modeling of Digital Signal Propagation in 3-D Circuits with Passive and Active Loads," *IEEE Trans. Microwave Theory Tech.*, vol.42, pp.1514-1523, 1994.

[6] K.S.Yee, "Numerical Solution of Initial Boundary Value Problems Involving Maxwell's Equation in Isotropic Media," *IEEE Trans. Antennas Propagation*, vol.14, pp.302-307, 1966.

[7] P.Antognetti and G.Massobrio eds., *Semiconductor Device Modeling with SPICE*, McGraw-Hill, New York, 1998, pp.143.

[8] Pacific Numerix Corp., *Parasitic Parameters and SPICE Link Technical Manual*, Arizona, 1994.